Q.P. Code: **16EC5704** **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
M.Tech I Year I Semester (R16) Regular Examinations January 2017
VERILOG HDL
(VLSI)
(For Students admitted in 2016 only)

Time: **3 hours** Max. Marks: **60**

(Answer all Five Units **5 X 12 =60** Marks)

UNIT-I

Q.1		Explain in detail about Verilog HDL data types with suitable examples.	12M

OR

Q.2	a.	Explain following concepts. a) Verilog strings b) Verilog constants c) Verilog operations d) Verilog variables.	7M
	b.	Write a brief notes on number representation in verilog.	5M

UNIT-II

Q.3	a.	What is user defined primitives? Explain combinational behavior of user defined primitives	7M
	b.	Explain conditional operator, operator precedence in VERILOG.	5M

OR

Q.4	a.	Explain following concepts with example program. a) Verilog operators b) Verilog variables.	7M
	b.	Explain the following i) Inertial Delay Effects ii) Pulse Rejection	5M

UNIT-III

Q.5	a.	Write a short note on intra assignment delay.	5M
	b.	Explain behavioral models of finite state machines.	7M

OR

Q.6	a.	Write short notes on Simultaneous Procedural Assignments.	7M
	b.	What is the differences between an initial behavior and an always behavior	5M

UNIT-IV

Q.7	a.	Explain the block in the logical synthesis.	7M
	b.	b) Discuss about RTL synthesis	5M

OR

Q.8	a.	Draw the flow chart for synthesis of loops explain each block?	7M
	b.	Write program for synthesis of multi cycle operations	5M

UNIT-V

Q.9	a.	Discuss about Ambiguous signals?	7M
	b.	Write a program for NMOS Three input NOR gate?	5M

OR

Q.10	a.	Explain the CMOS transmission gates with diagram?	7M
	b.	Explain the true table for switch level MOSFET Transistor module?	5M

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